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EXAMINER	
PAREKH, NITIN	

ART UNIT	PAPER NUMBER
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/473,305	Frutschy et al
Examiner	**Art Unit**
Nitin Parekh	2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Sep 26, 2002*.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1, 2, 4-7, 12-16, and 28-33* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1, 2, 4-7, 12-16, and 28-33* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). 9
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 28 is rejected under 35 U.S.C. 102(b) as being anticipated by Fjelstad et al (US Pat. 5812378).

Regarding claim 28, Fjelstad et al disclose a structure comprising a substrate contact between an IC substrate (68 in Fig. 5 and 6) and a multilayered circuit board substrate (21 in Fig. 5 and 6; Col. 9, line 60) for forming a non-reflow electrical contact (70/42 in Fig. 5 and 6) with a solder/metal ball/bump comprising:

- a recess/hole (36 in Fig. 5 and 6) defined by in the substrate by a surface extending into the substrate, and

- a conductive material (45/42 in Fig. 5 and 6) layered over the recess forming a void (36 in Fig. 5 and 6) therebetween

(Fig. 5 and 6; Col. 12, line 27- Col. 13, line 20).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 2, 4-7 and 29-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Buschbom (US Pat. 5834335) in view of Hembree et al (US Pat. 5931685), the admitted prior art (APA) and Scholz (US Pat. 5329423).

Regarding claim 1, Buschbom discloses a microelectronic component assembly/package (27 in Fig. 3) comprising:

- an integrated circuit (IC)/microelectronic device substrate/package having a first and second surfaces (IC 16 in Fig. 3) and the first surface including conventional ball grid array (BGA) contacts/pads and terminals/solder balls (conventional contacts/pads not shown by a numerical reference in Fig. 3; see conventional contacts 214 in Fig. 5 of the APA)
- a printed circuit board (PCB) substrate (PCB 12 in Fig. 3) having a first and second surface and including conventional pads/contacts on the first surface (20 in Fig. 3; Col. 3, line 5; Col. 4, line 44)

- solder balls (28 in Fig. 3) extending between the IC substrate and PCB contacts where the solder balls are attached to the respective contacts/pads (Fig. 3; Col. 3, line 28), and

- a compression mechanism/support structure for imparting pressure between the substrate and the PCB (23 in Fig. 3; Col. 3, line 45)

(Fig. 3; Col. 2, line 57- Col. 4, line 51).

Buschbom fails to specify the PCB substrate being a motherboard.

However, motherboard is a PCB which is used for specific functions. Buschbom's non-reflow contact structure covers generic applications of an electrical connection between the the IC and other substrates such as a PWB, circuit board, multichip module, sub-assembly, etc (Col. 2 and 5). The admitted prior art discloses attaching microelectronic devices to conventional carrier/substrates such as motherboard (pp. 1-3; Fig. 5), expansion card, etc.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate motherboard so that the desired connection density and routing can be achieved using the APA's substrate in Buschbom's assembly.

Regarding claims 2 and 4, the claim elements have been addressed in the rejection as explained above for claim 1.

Regarding claim 5, as explained above for claim 1, Buschbom in view of the APA teaches the motherboard/PCB contacts being conventional pads/contacts (24 in Fig. 3; Col. 3, line 5) but fails to specify:

a) the contacts comprising a recess defined by at least one sidewall extending into the substrate and the recess width and shape of the contacts being same as a diameter of the solder ball and a semispherical surface of same radius as that of the solder ball respectively, and

b) attaching the solder balls to the motherboard and forming the recess as claimed above in a) in the substrate

a) Hembree et al teach forming non-reflow solder ball contact comprising a flat pad (42A in Fig. 3A) or a recess defined by vertical sidewalls (40 in Fig. 3; Col. 5, line 40; Col. 5-8) extending into the substrate (26 in Fig. 3) and conductive material (42 in Fig. 3) layered in the recess (Fig. 3-3E; Fig. 6A-10A).

Hembree et al further teach selecting the size, shape (circular, oval, square, etc.), dimensions, etc. of the recess including the conductive material (40 /42 in Fig. 3) and diameter of the bump/ball such that the electrical contact within the recess can be

accomplished to compensate for the variation in the in the diameter/shape of the bump/ball with minimal bump deformation (Col. 5, line 39-66).

Furthermore, Hembree et al show the recess (Fig. 10A) where the width of the recess is substantially same as a diameter of the solder ball and the void is formed in the recess (Col. 9, line 30).

b) Scholz teaches forming the bumps/balls and recesses (24/28 in Fig. 1) interchangeably on IC substrate and PCB substrate respectively (10/12 in Fig. 1) or those (58/62 in Fig. 3) on PCB substrate and IC substrate respectively (52/46 in Fig. 3) to achieve the desired yield and defect level in fabrication (Col. 3 and 5).

Furthermore, the determination of parameters such as radius of the solder ball, shape/size/profile of the recess, thickness of the liner/conductive material, etc. in chip packaging and interconnection technology art is a subject of routine experimentation and optimization to achieve the desired alignment, connection/fit and overall package/ dimension ground rules.

Therefore, it would have been obvious to the person of ordinary skill in the art at the time invention was made to incorporate the elements a) and b) so that the surface connection, reliability and bonding strength can be improved using Hembree et al, APA and Scholz's structures in Buschbom's assembly.

Regarding claims 6, 7 and 29-31, the claim elements have been addressed in the rejection as explained above for claims 1 and 5.

5. Claims 12-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Buschbom (US Pat. 5834335) in view of Hembree et al (US Pat. 5931685), the admitted prior art (APA), Scholz (US Pat. 5329423), Hembree (US Pat. 5783461), Domadia et al (US Pat. 5949137) and Gililand et al (US Pat. 6137161).

Regarding claim 12, the claim elements have been addressed in the rejection as explained above for claim 1.

Regarding claim 13, Buschbom further discloses the compression mechanism/support structure comprising a composite frame/heat sink plate/heat slug surrounding the IC substrate (18/30 in Fig. 1 and 3; Col. 3) and retention devices comprising anchors but fails to specify using:

a) a backing plate/strip (strip 31 in Fig. 2) abutting the second surface with a plurality of retention devices comprising bolts and nuts retaining respective bolt, and

b) a resilient spacer extending between the thermal plate and the interposer substrate.

a) The APA (Fig. 5) discloses conventional compression mechanism/support structure comprising:

- a frame surrounding the substrate

- a backing plate abutting the motherboard

- a thermal plate extending over the frame and adjacent the substrate second surface, and

- a plurality of retention devices comprising a plurality of bolts and nuts extending through the backing plate, frame and thermal plate.

Domadia et al teach using a support structure where the plurality of retention devices having a plurality of conventional bolts (bolt 46 in Fig. 5 and 7) extending through the back of the substrate, stiffener/frame portion and thermal plate/heat dissipater (Fig. 5-7; Col. 4, line 40-Col. 6, line 48).

b) Hembree teaches using a resilient elastomeric spacer ring/washer spring (22 in Fig. 2; Col. 4, line 4) extending between the thermal plate and the microelectronic device/interposer substrate to enhance the support/compression mechanism.

Therefore, it would have been obvious to the person of ordinary skill in the art at the time invention was made to incorporate the elements a)-c) so that the desired force/pressure level can be achieved using the APA, Domadia et al and Hembree's teachings in Buschbom's assembly.

Regarding claim 14, the claim elements have been addressed in the rejections as explained above for claims 12 and 13.

Regarding claim 15, Buschbom further discloses an interposer substrate (14 in Fig. 1) having a first and second surfaces and the surfaces including conventional contacts/terminals (24/28 in Fig. 1) having the (IC)/microelectronic device being in electrical contact with the first surface of the interposer (Col. 2, line 53- Col. 4, line 18) but fails to disclose at least one solder ball being attached to the interposer and the PCB/motherboard first surface.

Gililand et al teaches using a microelectronic component assembly/package comprising a conventional interposer between an IC and a PWB (12 and 18 respectively in Fig. 1) where the interposer has conventional pads/contacts (25, 22, etc. in Fig. 1) and solder balls (28, 24, etc. in Fig. 1) on both surfaces which are being attached to the respective pads/contacts on the PWB and the IC (Col. 2, line 25- Col. 3, line 45).

Therefore, it would have been obvious to the person of ordinary skill in the art at the time invention was made to incorporate an interposer having at least one solder ball being attached between the first contact surface and the motherboard first surface so that the surface connection, bonding strength and grounding/signal connection can

be improved using the APA and Gililand et al's substrate structures in Buschbom's assembly.

Regarding claim 16, the claim elements have been addressed in the rejections as explained above for claims 12, 13 and 15.

6. Claims 32 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hembree et al (US Pat. 5931685) in view of Scholz (US Pat. 5329423).

Regarding claim 32, Hembree et al disclose forming a variety of non-reflow solder ball contact structures comprising:

- a recess defined by vertical sidewalls (40 in Fig. 3; Col. 5, line 40; Col. 5-8) extending into the substrate (26 in Fig. 3)

- a conductive material comprising plated metal (42 in Fig. 6A) and solder (12, 12A/B, etc. in Fig. 6A) layered/formed in and over the recess (Fig. 6A).

Hembree et al fail to specify the recess being semispherical in shape and a radius of the upper surface of the conductive material being substantially same as that of the solder ball.

However, Hembree et al further teach selecting the size, shape (circular, oval, square, etc.), dimensions, etc. of the recess including the conductive material (40 /42 in Fig. 3) and diameter of the bump/ball such that the electrical contact within the recess can be accomplished to compensate for the variation in the in the diameter/shape of the bump/ball with minimal bump deformation (Col. 5, line 39-66). Hembree et al show the recess (Fig. 10A) where the radius/width of the upper surface in the recess is substantially same as a radius/diameter of the solder ball (Col. 9, line 30).

Scholz teaches forming the bumps and recesses in the substrates (24/26/58/60 and 28/30/62/64 respectively in Fig. 1/2 and 3/4) where conductive material (38/40 and 58/66 respectively in Fig. 1/2 and 3/4) layered over the recess and the recesses having semispherical or trapezoidal shape are dimensioned to fit the radius/curvature of the tip portion of the contact bumps (Col. 4, line 20-65) and to provide the desired alignment.

Furthermore, the determination of parameters such as radius of the solder ball, shape/size/profile of the recess, thickness of the liner/conductive material, etc. in chip packaging and interconnection technology art is a subject of routine experimentation and optimization to achieve the desired alignment, connection/fit and overall package/ dimension ground rules.

Therefore, it would have been obvious to the person of ordinary skill in the art at the time invention was made to select the recess being semispherical in shape and the radius of the upper surface of the conductive material being substantially same as that

of the solder ball so that the surface connection, bonding strength and alignment can be improved using Scholz's structure in Hembree et al's substrate.

Regarding claim 33, Hembree et al further disclose using conventional resilient/elastomeric material (48 in Fig. 3D) disposed between the substrate and the conductive material layer to improve the cushion effect for the substrate contact (Col. 8, line 15-34).

Response to Arguments

7. Applicant's arguments filed on 09-26-02 have been fully considered but they are not persuasive.

A. Applicant contends that the solder balls referred in Fig. 3, 5A and 4-6 do not belong to Buschbom patent.

This error has been corrected indicating the solder balls 28 being in Fig. 3.

B. Applicant contends that the solder balls do not extend between the substrate and PCB but extend between the IC substrate and the interposer as shown in Fig. 1 and 2.

However, as explained in the previous office action (paper #15, page 3), Fig. 3 in Buschbom shows the solder balls (28 in Fig. 3) extending between the IC substrate and PCB (16 and 12 respectively in Fig. 3).

C. Applicant contends that Buschbom discloses a PWB substrate and a combination of Buschbom and the APA teaching a motherboard as the substrate is not proper.

However, as explained above for claim 1, it is conventional in the chip interconnection technology art to use substrates/carriers in a variety of configurations such as expansion card, PCB/motherboard, MCM card, etc. to achieve the desired interconnection/expansion requirements for different components and modules. Furthermore, the APA teaches attaching microelectronic devices to conventional carrier/substrates such as motherboard (pp. 1-3; Fig. 5), expansion card, etc. Therefore, APA's motherboard substrate is applied to Buschbom's assembly.

D. Applicant contends that Hembree et al and Hembree's non-reflow electrical contacts/design for temporary package do not apply to the microelectronic component assembly as claimed.

However, the assembly processes, bonding methods and materials used in assembly and fabrication of Hembree et al and Hembree's microelectronic components

of temporary package for functional testing and certification of a known good die of a package are those used in the conventional fabrication and assembly of microelectronic devices in chip packaging and interconnection technology art (Col. 4-12 and 3-8 respectively). Therefore, Hembree et al and Hembree's non-reflow electrical contacts design/teaching is applied to the above rejections.

Papers related to this application may be submitted directly to Art Unit 2811 by Facsimile transmission. Papers should be faxed to Art Unit via Tech Center 2800 fax center located in Crystal Plaza 4, Room 4C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh at (703) 305-3410. The examiner can normally be reached on Monday-Friday from 08:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (703) 308-2772. The fax number for the organization where this application or proceeding is assigned is (703) 308-7722 or 7724.

Nitin Parekh

12-12-02

Tom Thomas

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